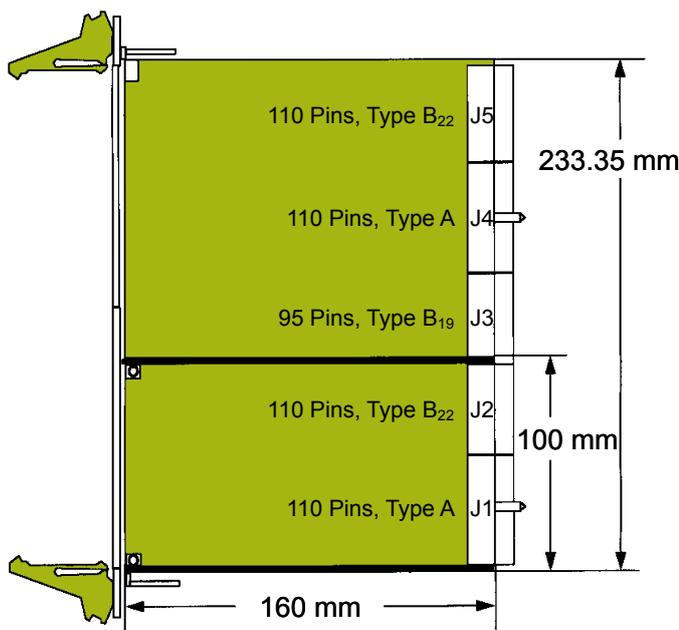


CompactPCI<sup>®</sup> as a standard is maintained and enhanced by the PCI Industrial Computer Manufacturers Group (PICMG<sup>®</sup>). It defines a combination of the electrical and logical specifications of the PCI standard and the mechanical specifications of the IEEE 1101 and IEC 60297 series of standards. The board connector has been developed from the IEC 61076-4-101 series of 2.0 mm connectors. The mounting location and dimensions for the 2.0 mm connectors are specified in IEEE 1101.11. Some additional mechanical definitions for 2.0 mm connectors in the Eurocard format are being specified in the VITA 30 draft.

Other international standards are listed in the CompactPCI<sup>®</sup> standard for environmental and

J1/P1 and J2/P2 as a minimum. Backplanes should always have the full complement of connectors to be compatible with any type of board.



As opposed to the CPCI standard (pins numbered from bottom to top), the contact numbers on the connector are numbered from top to bottom (according to the IEC standard).

The front panel of CPCI cards may be equipped with additional keying pegs to code individual board types. There is also an extended pin length to remove any electro static charge before contacts on the rear connectors mate. This pin also functions as a mechanical guide to position the board as straight as possible for insertion. This prevents pin bending and lowers the insertion force. Some applications could require up to 500 pins to be pushed into sockets simultaneously.

Connectors for high availability applications (hot swap) come with 3 different lengths of pins for a staged sequence of mate or break of contact.

related specifications. This gives CompactPCI<sup>®</sup> a solid foundation of international standards and practices for mechanical robustness.

The board format is either a 3U or a 6U Eurocard as defined in IEC 60297. There are two or five connectors specified for 3U or 6U boards respectively. Connectors are numbered from J1/P1 through J5/P5 (bottom to top) on the board or backplane. Slave or peripheral boards need J1/P1 as a minimum, master or system boards need both

Connector J1/P1 carries the signals for a 32 bit PCI bus (see table of contact assignments for J1/P1). Connector J2/P2 on a system card has the additional signals for a 64 bit PCI bus and some user-defined I/O (see table of contact assignments for J2/P2). On slave cards all of J2/P2 might be user-defined I/O except the top row which carries the signals for geographical addressing. J3/P3 should be reserved for other system bus definitions. J4/P4 and J5/P5 are used for I/O or secondary buses, e.g. H.110 in telecom applications or for bridges into other buses like VMEbus. This is used to accommodate two bus platforms in one card cage on one backplane.